

	L #	Hits	Search Text	DBs
1	L1	37	(detect\$3 near10 (invalid\$4 near10 (instruction opcode code))) .ab,ti.	USPAT; US-PGPUB
2	L2	2	((opcode instruction) near10 (valid\$4 invalid\$4 correct incorrect)) near50 (instruction near10 (select\$3 replac\$5 substitut\$3) near10 (nop noop no-op))	EPO; JPO; DERWENT; IBM_TDB
3	L3	10	((opcode instruction) near10 (valid\$4 invalid\$4 correct incorrect)) near50 (instruction near10 (select\$3 replac\$5 substitut\$3) near10 (nop noop no-op))	USPAT; US-PGPUB
4	L4	10	((opcode instruction) near10 (valid\$4 invalid\$4 correct incorrect)) near50 ((opcode instruction) near10 (select\$3 replac\$5 substitut\$3) near10 (nop noop no-op))	USPAT; US-PGPUB
5	L5	155	((detect\$3 determin\$3 check\$3 verif\$6 match\$3 compar\$3) near10 (opcode instruction) near10 (valid\$4 invalid\$4 correct incorrect)) near50 ((opcode instruction) near10 (select\$3 replac\$5 substitut\$3))	USPAT; US-PGPUB
6	L6	22	((detect\$3 determin\$3 check\$3 verif\$6 match\$3 compar\$3) near10 (opcode instruction) near10 (valid\$4 invalid\$4 correct incorrect)) near50 ((opcode instruction) near10 (select\$3 replac\$5 substitut\$3))	EPO; JPO; DERWENT; IBM_TDB

	L #	Hits	Search Text	DBs
1	L4	9505	instruction near10 (valid\$4 invalid\$4 correct incorrect)	USPAT; US-PGPUB
2	L5	224	instruction near10 (select\$3 replac\$5 substitut\$3) near10 (nop noop no-op)	USPAT; US-PGPUB
3	L6	10	4 near50 5	USPAT; US-PGPUB
4	L7	2752	instruction near10 (valid\$4 invalid\$4 correct incorrect)	EPO; JPO; DERWENT; IBM_TDB
5	L8	51	instruction near10 (select\$3 replac\$5 substitut\$3) near10 (nop noop no-op)	EPO; JPO; DERWENT; IBM_TDB
6	L9	2	7 near50 8	EPO; JPO; DERWENT; IBM_TDB

	Docum ent ID	U	Title	Current OR
1	US 20020 14417 6 A1	<input type="checkbox"/>	Method and apparatus for improving reliability in microprocessors	714/11
2	US 20020 14408 7 A1	<input type="checkbox"/>	Architecture of method for fetching microprocessor's instructions	712/207
3	US 55049 16 A	<input type="checkbox"/>	Digital signal processor with direct data transfer from external memory	712/36
4	US 54427 99 A	<input type="checkbox"/>	Digital signal processor with high speed multiplier means for double data input	712/36
5	US 54210 23 A	<input type="checkbox"/>	Motion vector calculation method using sequential minimum distortion calculations at different densities	348/701
6	US 54086 25 A	<input type="checkbox"/>	Microprocessor capable of decoding two instructions in parallel	712/210
7	US 53882 36 A	<input type="checkbox"/>	Digital signal processor with multiway branching based on parallel evaluation of N threshold values followed by sequential evaluation of M	712/236
8	US 52437 05 A	<input type="checkbox"/>	System for rapid return of exceptional processing during sequence operation instruction execution	712/228
9	US 51612 47 A	<input type="checkbox"/>	Digital signal processor matching data blocks against a reference block and replacing the reference block when a new minimum distortion block is calculated	712/36
10	US 50310 96 A	<input type="checkbox"/>	Method and apparatus for compressing the execution time of an instruction stream executing in a pipelined processor	711/169

	Docum ent ID	U	Title	Current OR
1	JP 20031 14796 A	<input type="checkbox"/>	COMPUTER CONTROL CIRCUIT	
2	JP 20021 96950 A	<input checked="" type="checkbox"/>	DEBUGGING SYSTEM	
3	JP 20020 07113 A	<input checked="" type="checkbox"/>	MICROPROCESSOR AND HOST COMPUTER AND REWRITING DEVICE	
4	JP 20012 90638 A	<input checked="" type="checkbox"/>	COMPUTER SYSTEM AND INSTRUCTION EXCHANGING METHOD	
5	JP 20000 81982 A	<input checked="" type="checkbox"/>	COMPILER, PROCESSOR AND RECORDING MEDIUM	
6	JP 11306 028 A	<input checked="" type="checkbox"/>	INSTRUCTION CACHE CONTROLLER AND RECORDING MEDIUM	
7	JP 11288 374 A	<input checked="" type="checkbox"/>	SIMULATOR FOR DIGITAL COMPUTER	
8	JP 11249 881 A	<input checked="" type="checkbox"/>	CONTROLLER	
9	JP 11149 390 A	<input checked="" type="checkbox"/>	DATA PROCESSOR AND FAULT DIAGNOSTIC METHOD IN THE SAME	
10	JP 10340 209 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	
11	JP 10254 695 A	<input checked="" type="checkbox"/>	MICROPROGRAM SPEED CONTROL CIRCUIT	
12	JP 08179 945 A	<input checked="" type="checkbox"/>	SIGNAL PROCESSOR	
13	JP 08069 340 A	<input checked="" type="checkbox"/>	METHOD AND DEVICE FOR MEASURING NUMBER OF CLOCK CYCLE	
14	JP 07295 694 A	<input checked="" type="checkbox"/>	POWER SAVING METHOD FOR ARITHMETIC PROCESSOR	
15	JP 06195 226 A	<input checked="" type="checkbox"/>	PROGRAM LOADING SYSTEM	
16	JP 05334 197 A	<input checked="" type="checkbox"/>	INSTRUCTION RAM UPDATING CIRCUIT	
17	JP 04361 328 A	<input checked="" type="checkbox"/>	PROCESSING MODE SWITCHING SYSTEM	
18	JP 04274 520 A	<input checked="" type="checkbox"/>	MICROPROGRAM CONTROLLER	
19	JP 04074 227 A	<input checked="" type="checkbox"/>	OPTIMIZATION SYSTEM FOR MACHINE WORD CODE	
20	JP 02132 545 A	<input checked="" type="checkbox"/>	PARALLEL COMPUTER AND ITS COMPILING METHOD	
21	JP 02081 237 A	<input checked="" type="checkbox"/>	CHECKING METHOD FOR USER PROGRAM OF ONE CHIP MICROCOMPUTER	

	Docum ent ID	U	Title	Current OR
22	JP 01253 032 A	<input checked="" type="checkbox"/>	MICROPROGRAM CONTROL TYPE PROCESSOR	
23	JP 01213 719 A	<input checked="" type="checkbox"/>	DATA REARRANGING DEVICE FOR PIPELINE PROCESSING	
24	JP 01211 135 A	<input checked="" type="checkbox"/>	PROGRAM DEBUGGING SYSTEM	
25	JP 63137 330 A	<input checked="" type="checkbox"/>	MICROPROGRAM CONTROLLER	
26	JP 63061 330 A	<input checked="" type="checkbox"/>	MICROPROGRAM CONTROL DEVICE	
27	JP 62254 238 A	<input checked="" type="checkbox"/>	COMPILING DEVICE	
28	JP 62010 736 A	<input checked="" type="checkbox"/>	PREFETCHING CONTROL SYSTEM FOR MICRO INSTRUCTION	
29	JP 61217 838 A	<input checked="" type="checkbox"/>	TEST METHOD OF MICROPROCESSOR	
30	JP 61213 929 A	<input checked="" type="checkbox"/>	DATA PROCESSING DEVICE WITH AUXILIARY PROCESSOR	
31	JP 61068 640 A	<input checked="" type="checkbox"/>	INSTRUCTION PROCESSING CIRCUIT OF MICROCOMPUTER	
32	JP 60105 048 A	<input checked="" type="checkbox"/>	MICROPROGRAM CONTROL SYSTEM	
33	JP 57210 497 A	<input checked="" type="checkbox"/>	ROM DATA INSPECTION SYSTEM	
34	JP 56169 451 A	<input checked="" type="checkbox"/>	DATA TRANSMISSION SYSTEM	
35	NNRD4 10118	<input checked="" type="checkbox"/>	Generic Methodology for Code Patching in Binary File	
36	NB901 1326	<input checked="" type="checkbox"/>	Masked Delayed Branches for Pipelined Computer Processors.	
37	JP 20031 14796 A	<input checked="" type="checkbox"/>	Computer control circuit, has selector for selecting No operation instruction code, when instruction code output from synchronous memory corresponds to jump command	
38	US 63743 46 B	<input checked="" type="checkbox"/>	Instruction execution method in microprocessor in digital system, involves comparing condition value in selected condition register with two different values for executing inspection or treating instructions as NOP	
39	JP 20010 15690 A	<input checked="" type="checkbox"/>	Large scale integrated system outputs initialization information corresponding to address value output by CPU to internal data bus, when selecting signal is invalid	
40	US 63145 10 B	<input checked="" type="checkbox"/>	Microprocessor has decoder that decodes modified nop instruction having dirty bit register field of selected dirty bit register and generates decoded signals	
41	JP 11306 028 A	<input checked="" type="checkbox"/>	Instruction cache control apparatus for memory access in reduced instruction set computer - has instruction generation unit that outputs pre-instruction to fetch and replace instruction address of predetermined line point with NOP instruction in present line	
42	JP 11249 881 A	<input checked="" type="checkbox"/>	Control apparatus e.g. programmable logic controller - has NOP instruction area and substituted objective program that are superscribed by substituted program, after NOP instruction area is distributed immediately after substituted objective program	

	Docum ent ID	U	Title	Current OR
43	EP 92659 6 A	<input checked="" type="checkbox"/>	Instruction reordering method for reducing processor power consumption	
44	JP 11149 390 A	<input checked="" type="checkbox"/>	Error detection method for calculator of data processor e.g. computer - involves comparing output of calculator with previous calculation result, stored in register, using comparator which outputs error signal when compared data are different	
45	JP 10161 875 A	<input checked="" type="checkbox"/>	Parallel data processor with calculator fault detection function - outputs fault detection signal showing calculator failure, based on comparison of calculation results using source operand and predetermined calculator	
46	RD 41011 8 A	<input checked="" type="checkbox"/>	Code patching for binary file e.g. for fixing Year-2000 omissions in all shipped product - locating patch code at end of code segment that requires modification, changing first instruction of original code into CALL instruction to activate patch code, and then replacing all of original code with no-operation instructions	
47	JP 09022 399 A	<input checked="" type="checkbox"/>	Parallel image processor with image memory and processor array - in which address of image memory designated by instruction in command latch is output to processor array, when instruction stored in command latch is memory access command	
48	JP 08179 945 A	<input checked="" type="checkbox"/>	Audio signal processing appts. for CD - has instruction ROM storing DSP arithmetic command, address control command, NOP command selection bit and NOP frequency display bit using which outputs of multiplier and adder are processed	
49	JP 07181 969 A	<input checked="" type="checkbox"/>	Code segment substitution device - has memory interface which stores new instructions in host memory after replacing current instructions into MSP memory after masking process	
50	US 53966 22 A	<input checked="" type="checkbox"/>	Radix sorting system using dynamic branch table - distributing contents of input bucket to several output buckets according to value of key field byte of present rank	
51	TW 20757 9 A	<input type="checkbox"/>	Microprocessor instructions pre-read and pre-decode method - involves storing adjacent instructions in odd and even buses and setting program counter value during decoding step before execution of next instruction	

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4	L4	10	((opcode instruction) near10 (valid\$4 invalid\$4 correct incorrect)) near50 ((opcode instruction) near10 (select\$3 replac\$5 substitut\$3) near10 (nop noop no-op))	USPAT; US-PGPUB
5	L6	22	((detect\$3 determin\$3 check\$3 verif\$6 match\$3 compar\$3) near10 (opcode instruction) near10 (valid\$4 invalid\$4 correct incorrect)) near50 ((opcode instruction) near10 (select\$3 replac\$5 substitut\$3))	EPO; JPO; DERWENT; IBM_TDB
6	L5	155	((detect\$3 determin\$3 check\$3 verif\$6 match\$3 compar\$3) near10 (opcode instruction) near10 (valid\$4 invalid\$4 correct incorrect)) near50 ((opcode instruction) near10 (select\$3 replac\$5 substitut\$3))	USPAT; US-PGPUB
7	L12	58	(detect\$3 near10 (invalid\$4 near10 (instruction opcode))).ab,ti.	EPO; JPO; DERWENT; IBM_TDB

	Docum ent ID	U	Title	Current OR
1	US 20030 19007 8 A1	<input type="checkbox"/>	Apparatus and method for detecting error in a digital image	382/232
2	US 20030 09552 1 A1	<input type="checkbox"/>	Device, system, method and computer readable medium for pairing of devices in a short distance wireless network	370/338
3	US 20020 07149 1 A1	<input type="checkbox"/>	Signal processor	375/240 .23
4	US 20020 07086 3 A1	<input type="checkbox"/>	Tagging system and method	340/572 .1
5	US 64418 10 B1	<input type="checkbox"/>	Telemetry encoding technique for smart stylus	345/179
6	US 61784 95 B1	<input type="checkbox"/>	Processor E-unit to I-unit interface instruction modification with E-unit opcode computer logic in the unit	712/209
7	US 61545 04 A	<input type="checkbox"/>	Encoding method, encoding apparatus, decoding method, decoding apparatus, and recording medium	375/265
8	US 61310 88 A	<input type="checkbox"/>	Electronic catalog system and method	705/27
9	US 60921 85 A	<input type="checkbox"/>	Opcode compare logic in E-unit for breaking infinite loops, detecting invalid opcodes and other exception checking	712/219
10	US 59616 33 A	<input type="checkbox"/>	Execution of data processing instructions	712/216
11	US 58812 79 A	<input type="checkbox"/>	Method and apparatus for handling invalid opcode faults via execution of an event-signaling micro-operation	712/244
12	US 58505 32 A	<input type="checkbox"/>	Invalid instruction scan unit for detecting invalid predecode data corresponding to instructions being fetched	712/213
13	US 58223 13 A	<input type="checkbox"/>	Seamless handover in a cordless TDMA system	370/332
14	US 58020 76 A	<input type="checkbox"/>	Audio error mitigation technique for a TDMA communication system	714/747
15	US 57548 64 A	<input type="checkbox"/>	Software piracy detection system	717/173
16	US 57455 04 A	<input type="checkbox"/>	Bit error resilient variable length code	714/752
17	US 56873 11 A	<input type="checkbox"/>	Microcomputer with detection of predetermined data for enabling execution of instructions for stopping supply of clock	714/34
18	US 56712 31 A	<input type="checkbox"/>	Method and apparatus for performing cache snoop testing on a cache system	714/724
19	US 56491 37 A	<input type="checkbox"/>	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/207
20	US 56128 84 A	<input type="checkbox"/>	Remote meter operation	705/403
21	US 55508 37 A	<input type="checkbox"/>	Adaptive differential pulse code modulation system with transmission error compensation	714/708



	Docum ent ID	U	Title	Current OR
22	US 55420 84 A	<input type="checkbox"/>	Method and apparatus for executing an atomic read-modify-write instruction	345/501
23	US 55111 75 A	<input type="checkbox"/>	Method an apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/216
24	US 54045 57 A	<input type="checkbox"/>	Data processor with plural instruction execution parts for synchronized parallel processing and exception handling	712/23
25	US 53694 01 A	<input type="checkbox"/>	Remote meter operation	705/403
26	US 53650 48 A	<input type="checkbox"/>	Bar code symbol reading apparatus with double-reading preventing function	235/462 .08
27	US 52261 30 A	<input type="checkbox"/>	Method and apparatus for store-into-instruction-stream detection and maintaining branch prediction cache consistency	712/238
28	US 48902 53 A	<input type="checkbox"/>	Predetermination of result conditions of decimal operations	708/525
29	US 48090 87 A	<input type="checkbox"/>	Apparatus for recording a discriminative signal	386/100
30	US 47992 55 A	<input type="checkbox"/>	Communication facilities access control arrangement	379/189
31	US 46461 67 A	<input type="checkbox"/>	Time code decoder	386/62
32	US 45814 88 A	<input type="checkbox"/>	Last number redial device	379/359
33	US 45089 39 A	<input type="checkbox"/>	Last number redial device	379/357 .04
34	US 42413 96 A	<input type="checkbox"/>	Tagged pointer handling apparatus	711/154
35	US 41677 78 A	<input type="checkbox"/>	Invalid instruction code detector	712/208
36	US 39407 62 A	<input type="checkbox"/>	Digital detection criteria control device for video mapping, detection parameter control, optimum radar receiver selection and rejection of non-moving targets	342/90
37	US 37709 00 A	<input type="checkbox"/>	AUDIO MULTIFREQUENCY SIGNAL RECEIVER	379/351

	Docum ent ID	U	Title	Current OR
1	US 20030 18254 0 A1	<input type="checkbox"/>	Method for limiting physical resource usage in a virtual tag allocation environment of a microprocessor	712/225
2	US 20030 18253 7 A1	<input checked="" type="checkbox"/>	Mechanism to assign more logical load/store tags than available physical registers in a microprocessor system	712/216
3	US 20030 17225 8 A1	<input checked="" type="checkbox"/>	Control forwarding in a pipeline digital processor	712/234
4	US 20030 14398 1 A1	<input checked="" type="checkbox"/>	Sequential presentation of long instructions in an interactive voice response system	455/414 .1
5	US 20030 13135 1 A1	<input checked="" type="checkbox"/>	Video system for integrating observer feedback with displayed images	725/24
6	US 20030 13122 0 A1	<input checked="" type="checkbox"/>	Bi-directional return register stack recovery from speculative execution of call/return upon branch misprediction	712/242
7	US 20030 10594 3 A1	<input checked="" type="checkbox"/>	Mechanism for processing speculative LL and SC instructions in a pipelined processor	712/216
8	US 20030 09377 1 A1	<input checked="" type="checkbox"/>	Debugging aid device, a compiling device, a debugging aid program, a compiling program, and a computer readable record medium therefor	717/125
9	US 20030 09249 2 A1	<input checked="" type="checkbox"/>	Game system, game control method, and recording medium for the same	463/42
10	US 20030 07006 2 A1	<input checked="" type="checkbox"/>	System and method for reducing computing system latencies associated with branch instructions	712/234
11	US 20030 04385 8 A1	<input checked="" type="checkbox"/>	Device for processing data signals, method thereof, and device for multiplexing data signals	370/537
12	US 20030 03722 5 A1	<input checked="" type="checkbox"/>	Apparatus and method for microcontroller debugging	712/227
13	US 20020 18883 4 A1	<input checked="" type="checkbox"/>	Apparatus and method for target address replacement in speculative branch target address cache	712/238
14	US 20020 15708 4 A1	<input checked="" type="checkbox"/>	Method and system for displaying translation information	717/141
15	US 20020 15199 2 A1	<input checked="" type="checkbox"/>	Media recording device with packet data interface	700/83
16	US 20020 12416 2 A1	<input checked="" type="checkbox"/>	Computer system and method for fetching a next instruction	712/238
17	US 20020 10429 3 A1	<input checked="" type="checkbox"/>	Packaging system	53/472

	Docum ent ID	U	Title	Current OR
18	US 20020 09545 9 A1	<input checked="" type="checkbox"/>	Method and apparatus for providing a client by a server with an instruction data set in a predetermined format in response to a content data request message by a client	709/203
19	US 20020 08331 2 A1	<input checked="" type="checkbox"/>	Branch Prediction apparatus and process for restoring replaced branch history for use in future branch predictions for an executing program	712/240
20	US 20020 06937 5 A1	<input checked="" type="checkbox"/>	System, method, and article of manufacture for data transfer across clock domains	713/400
21	US 20020 03075 1 A1	<input checked="" type="checkbox"/>	Image control device with information-based image correcting capability, image control method and digital camera	348/222 .1
22	US 20020 01085 1 A1	<input checked="" type="checkbox"/>	Emulated branch effected by trampoline mechanism	712/244
23	US 20010 01876 4 A1	<input checked="" type="checkbox"/>	Method and apparatus for translating between source and target code	717/146
24	US 20010 01694 1 A1	<input checked="" type="checkbox"/>	Method for translating between source and target code with heterogenous register sets	717/141
25	US 20010 01694 0 A1	<input checked="" type="checkbox"/>	System and method for translating include files	717/141
26	US 20010 01687 0 A1	<input checked="" type="checkbox"/>	Method for at least making ready for mailing at least one message, and data structure for use therein	709/203
27	US 20010 01308 6 A1	<input checked="" type="checkbox"/>	Multiprocessor system and data transmitting method	711/119
28	US 66314 60 B1	<input checked="" type="checkbox"/>	Advanced load address table entry invalidation based on register address wraparound	712/217
29	US 65948 21 B1	<input checked="" type="checkbox"/>	Translation consistency checking for modified target instructions by comparing to original copy	717/136
30	US 65606 96 B1	<input checked="" type="checkbox"/>	Return register stack target predictor	712/237
31	US 65500 02 B1	<input checked="" type="checkbox"/>	Method and system for detecting a flush of an instruction without a flush indicator	712/216
32	US 65500 01 B1	<input checked="" type="checkbox"/>	Method and implementation of statistical detection of read after write and write after write hazards	712/216
33	US 65131 09 B1	<input checked="" type="checkbox"/>	Method and apparatus for implementing execution predicates in a computer processing system	712/200
34	US 65052 96 B2	<input checked="" type="checkbox"/>	Emulated branch effected by trampoline mechanism	712/244
35	US 64776 41 B2	<input checked="" type="checkbox"/>	Method for translating between source and target code with heterogenous register sets	712/241
36	US 64776 39 B1	<input checked="" type="checkbox"/>	Branch instruction mechanism for processor	712/237

	Docum ent ID	U	Title	Current OR
37	US 64571 75 B1	<input checked="" type="checkbox"/>	Method and apparatus for installing a software upgrade within a memory resource associated with a computer system	717/173
38	US 64567 77 B1	<input checked="" type="checkbox"/>	Information processor, information processing method and information recording medium on which information processing method is recorded	386/46
39	US 64461 97 B1	<input checked="" type="checkbox"/>	Two modes for executing branch instructions of different lengths and use of branch control instruction and register set loaded with target instructions	712/237
40	US 64184 24 B1	<input checked="" type="checkbox"/>	Ergonomic man-machine interface incorporating adaptive pattern recognition based control system	706/21
41	US 64009 96 B1	<input checked="" type="checkbox"/>	Adaptive pattern recognition based control system and method	700/83
42	US 63895 31 B1	<input checked="" type="checkbox"/>	Indexing branch target instruction memory using target address generated by branch control instruction to reduce branch latency	712/237
43	US 63743 70 B1	<input checked="" type="checkbox"/>	Method and system for flexible control of BIST registers based upon on-chip events	714/39
44	US 63743 48 B1	<input checked="" type="checkbox"/>	Prioritized pre-fetch/preload mechanism for loading and speculative preloading of candidate branch target instruction	712/237
45	US 63569 97 B1	<input checked="" type="checkbox"/>	Emulating branch instruction of different instruction set in a mixed instruction stream in a dual mode system	712/237
46	US 63246 43 B1	<input checked="" type="checkbox"/>	Branch prediction and target instruction control for processor	712/237
47	US 63082 58 B1	<input checked="" type="checkbox"/>	Data processing circuit with target instruction and prefix instruction	712/210
48	US 63049 61 B1	<input checked="" type="checkbox"/>	Computer system and method for fetching a next instruction	712/238
49	US 62725 61 B1	<input checked="" type="checkbox"/>	Sound blaster interface card auto-detection method	710/8
50	US 62533 74 B1	<input checked="" type="checkbox"/>	Method for validating a signed program prior to execution time or an unsigned program at execution time	717/126
51	US 62533 17 B1	<input checked="" type="checkbox"/>	Method and apparatus for providing and handling traps	712/244
52	US 62471 23 B1	<input checked="" type="checkbox"/>	Branch prediction mechanism employing branch selectors to select a branch prediction	712/239
53	US 61856 76 B1	<input checked="" type="checkbox"/>	Method and apparatus for performing early branch prediction in a microprocessor	712/239
54	US 61856 74 B1	<input checked="" type="checkbox"/>	Method and apparatus for reconstructing the address of the next instruction to be completed in a pipelined processor	712/230
55	US 61675 05 A	<input checked="" type="checkbox"/>	Data processing circuit with target instruction and prefix instruction	712/210
56	US 61674 60 A	<input checked="" type="checkbox"/>	System for replacing control information in a printer according to external instruction information if a replacement function is valid	710/5
57	US 60817 50 A	<input checked="" type="checkbox"/>	Ergonomic man-machine interface incorporating adaptive pattern recognition based control system	700/17
58	US 60773 12 A	<input checked="" type="checkbox"/>	Apparatus, program product and method of debugging utilizing a context sensitive breakpoint	717/129
59	US 60598 40 A	<input checked="" type="checkbox"/>	Automatic scheduling of instructions to reduce code size	717/154

	Docum ent ID	U	Title	Current OR
60	US 60592 25 A	<input checked="" type="checkbox"/>	Flight control device for an aircraft, in particular a helicopter	244/17. 13
61	US 60498 60 A	<input checked="" type="checkbox"/>	Pipelined floating point stores	712/25
62	US 60354 26 A	<input checked="" type="checkbox"/>	System for memory error checking in an executable	714/54
63	US 60330 74 A	<input checked="" type="checkbox"/>	Subjective eye refractive power measuring apparatus	351/212
64	US 60235 61 A	<input checked="" type="checkbox"/>	System for processing traceable cache trace information	714/45
65	US 60147 28 A	<input checked="" type="checkbox"/>	Organization of an integrated cache unit for flexible usage in supporting multiprocessor operations	711/133
66	US 60121 25 A	<input checked="" type="checkbox"/>	Superscalar microprocessor including a decoded instruction cache configured to receive partially decoded instructions	711/125
67	US 60095 39 A	<input checked="" type="checkbox"/>	Cross-triggering CPUs for enhanced test operations in a multi-CPU computer system	714/30
68	US 60031 07 A	<input checked="" type="checkbox"/>	Circuitry for providing external access to signals that are internal to an integrated circuit chip package	710/316
69	US 59833 37 A	<input checked="" type="checkbox"/>	Apparatus and method for patching an instruction by providing a substitute instruction or instructions from an external memory responsive to detecting an opcode of the instruction	712/32
70	US 59745 43 A	<input checked="" type="checkbox"/>	Apparatus and method for performing subroutine call and return operations	712/240
71	US 59648 69 A	<input checked="" type="checkbox"/>	Instruction fetch mechanism with simultaneous prediction of control-flow instructions	712/236
72	US 59648 62 A	<input checked="" type="checkbox"/>	Execution unit and method for using architectural and working register files to reduce operand bypasses	712/23
73	US 59564 77 A	<input checked="" type="checkbox"/>	Method for processing information in a microprocessor to facilitate debug and performance monitoring	714/30
74	US 59564 76 A	<input checked="" type="checkbox"/>	Circuitry and method for detecting signal patterns on a bus using dynamically changing expected patterns	714/30
75	US 59499 72 A	<input checked="" type="checkbox"/>	System for memory error checking in an executable	714/54
76	US 59480 98 A	<input checked="" type="checkbox"/>	Execution unit and method for executing performance critical and non-performance critical arithmetic instructions in separate pipelines	712/221
77	US 59400 74 A	<input checked="" type="checkbox"/>	Remote upgrade of software over a network	345/749
78	US 59352 38 A	<input checked="" type="checkbox"/>	Selection from multiple fetch addresses generated concurrently including predicted and actual target by control-flow instructions in current and previous instruction bundles	712/206
79	US 59238 62 A	<input checked="" type="checkbox"/>	Processor that decodes a multi-cycle instruction into single-cycle micro-instructions and schedules execution of the micro-instructions	712/208
80	US 59208 90 A	<input checked="" type="checkbox"/>	Distributed tag cache memory system and method for storing data in the same	711/144
81	US 59012 46 A	<input checked="" type="checkbox"/>	Ergonomic man-machine interface incorporating adaptive pattern recognition based control system	382/209

	Docum ent ID	U	Title	Current OR
82	US 58872 43 A	<input checked="" type="checkbox"/>	Signal processing apparatus and methods	725/136
83	US 58870 03 A	<input checked="" type="checkbox"/>	Apparatus and method for comparing a group of binary fields with an expected pattern to generate match results	714/736
84	US 58812 79 A	<input checked="" type="checkbox"/>	Method and apparatus for handling invalid opcode faults via execution of an event-signaling micro-operation	712/244
85	US 58812 24 A	<input checked="" type="checkbox"/>	Apparatus and method for tracking events in a microprocessor that can retire more than one instruction during a clock cycle	714/47
86	US 58812 17 A	<input checked="" type="checkbox"/>	Input comparison circuitry and method for a programmable state machine	714/30
87	US 58806 71 A	<input checked="" type="checkbox"/>	Flexible circuitry and method for detecting signal patterns on a bus	340/146 .2
88	US 58751 08 A	<input checked="" type="checkbox"/>	Ergonomic man-machine interface incorporating adaptive pattern recognition based control system	700/17
89	US 58729 47 A	<input checked="" type="checkbox"/>	Instruction classification circuit configured to classify instructions into a plurality of instruction types prior to decoding said instructions	712/213
90	US 58676 44 A	<input checked="" type="checkbox"/>	System and method for on-chip debug support and performance monitoring in a microprocessor	714/39
91	US 58484 33 A	<input checked="" type="checkbox"/>	Way prediction unit and a method for operating the same	711/137
92	US 57649 46 A	<input checked="" type="checkbox"/>	Superscalar microprocessor employing a way prediction unit to predict the way of an instruction fetch address and to concurrently provide a branch prediction address corresponding to the fetch address	712/239
93	US 57646 24 A	<input checked="" type="checkbox"/>	Arm switching system and path changing method	370/218
94	US 57489 78 A	<input checked="" type="checkbox"/>	Byte queue divided into multiple subqueues for optimizing instruction selection logic	712/23
95	US 57404 18 A	<input checked="" type="checkbox"/>	Pipelined processor carrying out branch prediction by BTB	712/239
96	US 57377 49 A	<input checked="" type="checkbox"/>	Method and system for dynamically sharing cache capacity in a microprocessor	711/123
97	US 57297 07 A	<input checked="" type="checkbox"/>	Instruction prefetch circuit and cache device with branch detection	712/207
98	US 57175 87 A	<input checked="" type="checkbox"/>	Method and system for recording noneffective instructions within a data processing system	700/2
99	US 56447 79 A	<input checked="" type="checkbox"/>	Processing system and method of operation for concurrent processing of branch instructions with cancelling of processing of a branch instruction	712/23
100	US 56279 92 A	<input checked="" type="checkbox"/>	Organization of an integrated cache unit for flexible usage in supporting microprocessor operations	711/133
101	US 56194 08 A	<input checked="" type="checkbox"/>	Method and system for recoding noneffective instructions within a data processing system	712/226
102	US 55817 74 A	<input checked="" type="checkbox"/>	Data processor decoding and executing a train of instructions of variable length at increased speed	712/210
103	US 55487 39 A	<input checked="" type="checkbox"/>	Method and apparatus for rapidly retrieving data from a physically addressed data storage structure using address page crossing predictive annotations	711/204

	Docum ent ID	U	Title	Current OR
104	US 55354 05 A	<input checked="" type="checkbox"/>	Microsequencer bus controller system	710/110
105	US 55242 24 A	<input checked="" type="checkbox"/>	System for speculatively executing instructions wherein mispredicted instruction is executed prior to completion of branch processing	712/219
106	US 55009 42 A	<input checked="" type="checkbox"/>	Method of indicating parallel execution compoundability of scalar instructions based on analysis of presumed instructions	712/210
107	US 54796 16 A	<input checked="" type="checkbox"/>	Exception handling for prefetched instruction bytes using valid bits to identify instructions that will cause an exception	712/212
108	US 54559 38 A	<input checked="" type="checkbox"/>	Network based machine instruction generator for design verification	716/5
109	US 54406 96 A	<input checked="" type="checkbox"/>	Data processing device for reducing the number of internal bus lines	710/305
110	US 54328 49 A	<input checked="" type="checkbox"/>	Secure cryptographic operations using control vectors generated inside a cryptographic facility	380/280
111	US 54086 25 A	<input checked="" type="checkbox"/>	Microprocessor capable of decoding two instructions in parallel	712/210
112	US 53554 61 A	<input checked="" type="checkbox"/>	Method of and apparatus for selecting an origin address for use in translating a logical address in one of a plurality of virtual address spaces to a real address in a real address space	711/203
113	US 53534 26 A	<input checked="" type="checkbox"/>	Cache miss buffer adapted to satisfy read requests to portions of a cache fill in progress without waiting for the cache fill to complete	711/118
114	US 53534 21 A	<input checked="" type="checkbox"/>	Multi-prediction branch prediction mechanism	712/240
115	US 53352 77 A	<input checked="" type="checkbox"/>	Signal processing apparatus and methods	380/242
116	US 53193 62 A	<input checked="" type="checkbox"/>	Security system with security access database distributed among individual access devices	340/5.3 3
117	US 52972 55 A	<input checked="" type="checkbox"/>	Parallel computer comprised of processor elements having a local memory and an enhanced data transfer mechanism	712/14
118	US 52895 88 A	<input checked="" type="checkbox"/>	Interlock acquisition for critical code section execution in a shared memory common-bus individually cached multiprocessor system	711/120
119	US 52838 73 A	<input checked="" type="checkbox"/>	Next line prediction apparatus for a pipelined computed system	712/207
120	US 52768 53 A	<input checked="" type="checkbox"/>	Cache system	711/131
121	US 52437 05 A	<input checked="" type="checkbox"/>	System for rapid return of exceptional processing during sequence operation instruction execution	712/228
122	US 52336 54 A	<input checked="" type="checkbox"/>	Signal processing apparatus and methods	725/135
123	US 52221 22 A	<input checked="" type="checkbox"/>	Payphone having master and slave modes	379/32. 04
124	US 52068 23 A	<input checked="" type="checkbox"/>	Apparatus to perform Newton iterations for reciprocal and reciprocal square root	708/502
125	US 51858 78 A	<input checked="" type="checkbox"/>	Programmable cache memory as well as system incorporating same and method of operating programmable cache memory	711/123

	Docum ent ID	U	Title	Current OR
126	US 51670 26 A	<input checked="" type="checkbox"/>	Simultaneously or sequentially decoding multiple specifiers of a variable length pipeline instruction based on detection of modified value of specifier registers	712/210
127	US 51485 28 A	<input checked="" type="checkbox"/>	Method and apparatus for simultaneously decoding three operands in a variable length instruction when one of the operands is also of variable length	712/210
128	US 51426 33 A	<input checked="" type="checkbox"/>	Preprocessing implied specifiers in a pipelined processor	712/225
129	US 51366 91 A	<input checked="" type="checkbox"/>	Methods and apparatus for caching interlock variables in an integrated cache memory	711/139
130	US 51290 75 A	<input checked="" type="checkbox"/>	Data processor with on-chip logical addressing and off-chip physical addressing	711/169
131	US 51094 14 A	<input checked="" type="checkbox"/>	Signal processing apparatus and methods	725/135
132	US 50758 49 A	<input checked="" type="checkbox"/>	Information processor providing enhanced handling of address-conflicting instructions during pipeline processing	711/200
133	US 50310 96 A	<input checked="" type="checkbox"/>	Method and apparatus for compressing the execution time of an instruction stream executing in a pipelined processor	711/169
134	US 50253 66 A	<input checked="" type="checkbox"/>	Organization of an integrated cache unit for flexible usage in cache system design	711/128
135	US 49723 17 A	<input checked="" type="checkbox"/>	Microprocessor implemented data processing system capable of emulating execution of special instructions not within the established microprocessor instruction set by switching access from a main store portion of a memory	712/227
136	US 49658 25 A	<input checked="" type="checkbox"/>	Signal processing apparatus and methods	380/233
137	US 48274 02 A	<input checked="" type="checkbox"/>	Branch advanced control apparatus for advanced control of a branch instruction in a data processing system	712/234
138	US 48005 63 A	<input checked="" type="checkbox"/>	Error processing method and apparatus for information processing system	714/6
139	US 47915 57 A	<input checked="" type="checkbox"/>	Apparatus and method for monitoring and controlling the prefetching of instructions by an information processing system	712/244
140	US 46655 01 A	<input checked="" type="checkbox"/>	Workstation for local and remote data processing	710/8
141	US 46427 71 A	<input checked="" type="checkbox"/>	Diagnostic processing system for automatic transmission of an automobile	701/62
142	US 46281 93 A	<input checked="" type="checkbox"/>	Code reading operations supervisor	235/375
143	US 46176 25 A	<input checked="" type="checkbox"/>	Vector processor	712/4
144	US 45311 98 A	<input checked="" type="checkbox"/>	Operation mode monitor for microcomputer	714/23
145	US 45244 15 A	<input checked="" type="checkbox"/>	Virtual machine data processor	714/21
146	US 44882 28 A	<input checked="" type="checkbox"/>	Virtual memory data processor	714/21
147	US 44183 33 A	<input checked="" type="checkbox"/>	Appliance control system	340/310 .01



	Docum ent ID	U	Title	Current OR
148	US 44085 54 A	<input checked="" type="checkbox"/>	Automatic needle thread control apparatus	112/302
149	US 43685 34 A	<input checked="" type="checkbox"/>	Keyboard controlled vital digital communication system	714/807
150	US 42310 89 A	<input checked="" type="checkbox"/>	Data processing system with apparatus for correcting microinstruction errors	714/7
151	US 42107 85 A	<input checked="" type="checkbox"/>	Tape replay system	360/72. 2
152	US 41764 60 A	<input checked="" type="checkbox"/>	Opto-mechanical measuring system	33/504
153	US 41363 83 A	<input checked="" type="checkbox"/>	Microprogrammed, multipurpose processor having controllable execution speed	712/221
154	US 39449 86 A	<input checked="" type="checkbox"/>	Vehicle movement control system for railroad terminals	104/88. 04
155	US 38511 52 A	<input type="checkbox"/>	READ-OUT DATA ENTRY SYSTEM FOR A PLURALITY OF SUPER-IMPOSED DATA ENTRY CARDS	235/435

	Docum ent ID	U	Title	Current OR
1	JP 20022 43279 A	<input type="checkbox"/>	COMBUSTION CONTROLLER	
2	JP 20011 68772 A	<input checked="" type="checkbox"/>	DEVICE AND METHOD FOR SWITCHING HOT STANDBY LINE	
3	JP 20011 54877 A	<input checked="" type="checkbox"/>	DEVICE AND METHOD FOR CONTROLLING INTERRUPTION	
4	JP 10083 301 A	<input checked="" type="checkbox"/>	PARALLEL PROCESSOR	
5	JP 07200 294 A	<input checked="" type="checkbox"/>	PROCESSOR DEVICE PROVIDED WITH DELAY BRANCH EXECUTION FUNCTION	
6	JP 06168 263 A	<input checked="" type="checkbox"/>	VECTOR PROCESSOR	
7	JP 06110 784 A	<input checked="" type="checkbox"/>	MICROPROCESSOR DEVICE	
8	JP 06095 862 A	<input checked="" type="checkbox"/>	INSTRUCTION STRING OPTIMIZATION SUPPORTING DEVICE	
9	JP 06095 614 A	<input checked="" type="checkbox"/>	DISPLAY DEVICE	
10	JP 05346 890 A	<input checked="" type="checkbox"/>	DATA INVALIDATION CONTROL SYSTEM	
11	JP 05224 930 A	<input checked="" type="checkbox"/>	DATA PROCESSOR PROVIDED WITH PLURAL INSTRUCTION EXECUTING PARTS	
12	JP 04333 928 A	<input checked="" type="checkbox"/>	LSI CONTROL SYSTEM	
13	JP 04324 193 A	<input checked="" type="checkbox"/>	ELECTRICALLY PROGRAMMABLE READ ONLY MEMORY ATTACHED WITH WRITE PROTECTION	
14	JP 04182 735 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
15	JP 04177 440 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	
16	JP 04081 959 A	<input checked="" type="checkbox"/>	INPUT/OUTPUT INSTRUCTION CONTROL SYSTEM	
17	JP 04055 940 A	<input checked="" type="checkbox"/>	MICROPROGRAM CONTROL SYSTEM	
18	JP 04025 953 A	<input checked="" type="checkbox"/>	CACHE MEMORY ERROR PROCESSING SYSTEM	
19	JP 03296 111 A	<input checked="" type="checkbox"/>	OPERATION CONTROLLER FOR UNMANNED CARRIER	
20	JP 03211 622 A	<input checked="" type="checkbox"/>	INFORMATION PROCESSOR	
21	JP 03209 523 A	<input checked="" type="checkbox"/>	DETECTION SYSTEM FOR ERROR OF INSTRUCTION DATA	
22	JP 03142 533 A	<input checked="" type="checkbox"/>	CHECK SYSTEM FOR DECIMAL DATA	

	Docum ent ID	U	Title	Current OR
23	JP 03095 676 A	<input checked="" type="checkbox"/>	BACK-UP DEVICE FOR VERIFICATION OF SIMULATION RESULT	
24	JP 02235 151 A	<input checked="" type="checkbox"/>	DETECTING/CORRECTING SYSTEM FOR INVALID DATA IN PROGRAM EXECUTION	
25	JP 02208 743 A	<input checked="" type="checkbox"/>	DATA PROCESSOR	
26	JP 02029 850 A	<input checked="" type="checkbox"/>	TIGHT COUPLING PROCESSORS	
27	JP 01307 851 A	<input checked="" type="checkbox"/>	STORAGE CONTROL SYSTEM	
28	JP 01224 739 A	<input checked="" type="checkbox"/>	MICROCAMERA	
29	JP 01193 939 A	<input checked="" type="checkbox"/>	SYSTEM FOR CONTROLLING INSTRUCTION FETCH	
30	JP 01076 353 A	<input checked="" type="checkbox"/>	CONTROL SYSTEM FOR INPUT/OUTPUT INSTRUCTION	
31	JP 63244 153 A	<input checked="" type="checkbox"/>	MEMORY PROTECTING METHOD	
32	JP 63070 343 A	<input checked="" type="checkbox"/>	MICROCOMPUTER	
33	JP 63026 088 A	<input checked="" type="checkbox"/>	VIDEO FLOPPY REPRODUCING DEVICE	
34	JP 61294 553 A	<input checked="" type="checkbox"/>	INSTRUCTION PROCESSING SYSTEM	
35	JP 61015 235 A	<input checked="" type="checkbox"/>	CENTRAL PROCESSOR	
36	JP 60083 149 A	<input checked="" type="checkbox"/>	COMPUTER	
37	JP 58035 647 A	<input checked="" type="checkbox"/>	APPRECIATING DEVICE FOR MICROCOMPUTER	
38	GB 22822 45 A	<input checked="" type="checkbox"/>	Aborting execution of instructions.	
39	EP 34336 3 A2	<input checked="" type="checkbox"/>	Motor control system.	
40	US 65429 87 B	<input checked="" type="checkbox"/>	Instruction queue status detection method in pipelined computer architecture, involves subtracting number of enqueued instructions from sum of number of free rows and issued instructions, to determine number of free rows in specific cycle	
41	GB 23790 57 A	<input checked="" type="checkbox"/>	Memory operations testing method for computer program development detects accesses to unmapped region of two-region virtual memory associated with physical memory	
42	US 61192 04 A	<input checked="" type="checkbox"/>	Translation lookaside buffer coherency maintenance involves continuing processing of instructions in interval between receipt of synchronization request and sending of indication to first processor	
43	US 58812 79 A	<input checked="" type="checkbox"/>	Invalid opcode fault handling method for reduced instruction set (RISC) microprocessors used in computer system	

	Docum ent ID	U	Title	Current OR
44	US 58505 32 A	<input checked="" type="checkbox"/>	Invalid instruction scanner for superscalar microprocessor - has invalid instruction scan unit that detects invalid predecode information and identifies specific byte through invalid instruction pointer	
45	JP 10322 411 A	<input checked="" type="checkbox"/>	Data communication control apparatus for motor vehicle - has invalid processors provided for received data, which include control instructions for other apparatuses in motor vehicle, when latch signal and clock signal are not detected	
46	US 56689 84 A	<input checked="" type="checkbox"/>	Floating point processing system - detecting if operand is in valid form while being loaded into pipeline, staging execution of instruction when operand is invalid, converting operand to valid form, and using gate to present converted operand to pipeline after one delay stag	
47	US 54796 16 A	<input checked="" type="checkbox"/>	Exception handling system for prefetched instruction bytes in pipelined 486-type microprocessor - stores prefetched instruction byte in queue with valid bit if byte is invalid, when exception occurs, and detects if stall condition results from exception associated with prefetched instruction byte by checking stored instruction status	
48	JP 07252 031 A	<input checked="" type="checkbox"/>	Hall call registration device for lift system - has multiplication scene call button which registers call based on detected guest, and invalidates prior instruction after lift door opens at correct floor	
49	JP 07200 294 A	<input checked="" type="checkbox"/>	Pipeline processor with delay branch execution function - has command execution unit that executes delay branch instruction after completion of exception processing started by exception processing unit	
50	US 54045 57 A	<input checked="" type="checkbox"/>	Data processor - has instruction execution parts for synchronised parallel processing which generates order of each group of instructions having successive addresses and order of each instruction in each group of instructions	
51	EP 72161 9 B	<input checked="" type="checkbox"/>	Processing appts. for data stored in RAM - has conditional controller responding to memory access and condition test circuitry to prevent completion of current instruction on instruction error	
52	EP 46923 9 A	<input checked="" type="checkbox"/>	Detection and correction appts. for faulty processor operational codes - detects faulty instructions using logic nor circuit and replaces them with error-free micro-code from programmable array	
53	US 52261 30 A	<input checked="" type="checkbox"/>	Branch prediction cache with maintained consistency - organises store into instruction stream detection resulting in invalidation of corresponding cache entry data and main memory access	
54	US 49425 25 A	<input checked="" type="checkbox"/>	Data processor for concurrent executing of instructions - comprises instruction control circuit for decoding M instructions and reading operands in parallel, detection circuit and reserve circuit	
55	EP 15527 5 B	<input checked="" type="checkbox"/>	Data processor with instruction execution unit - has n-stage pipeline for providing data segments representing instruction words from memory to execution unit	
56	EP 98169 A	<input checked="" type="checkbox"/>	Data processing system providing performance measurement - uses interruption of timer for triggering performance measurement and stores results of processing of each measurement item	
57	EP 66376 A	<input checked="" type="checkbox"/>	Data processing system with instruction buffer - pre-transfers instructions from main storage to buffer which is invalidated only when changed content is executed as instruction	
58	US 41677 78 A	<input type="checkbox"/>	Invalid instruction code detector for digital computer - has RAM with flag indicating whether a particular combination of operation code bits is valid	

	Docum ent ID	U	Title	Current OR
1	JP 20023 14519 A	<input type="checkbox"/>	BIT SYNCHRONIZING CIRCUIT	
2	JP 20002 98587 A	<input checked="" type="checkbox"/>	PROCESSOR HAVING DEVICE BRANCHED TO SPECIFIED PARTY DURING INSTRUCTION REPETITION	
3	JP 10228 399 A	<input checked="" type="checkbox"/>	PARTIAL FILE UPDATING DEVICE	
4	JP 08137 687 A	<input checked="" type="checkbox"/>	PROGRAM CONTROLLER	
5	JP 06089 174 A	<input checked="" type="checkbox"/>	COMPUTER MEMORY SYSTEM	
6	JP 05127 720 A	<input checked="" type="checkbox"/>	OFFLINE INSTRUCTION DEVICE FOR ROBOT	
7	JP 05035 175 A	<input checked="" type="checkbox"/>	EDUCATIONAL SYSTEM	
8	JP 04283 856 A	<input checked="" type="checkbox"/>	DOCUMENT PROCESSOR	
9	JP 62242 104 A	<input checked="" type="checkbox"/>	CONTROL DEVICE FOR RUNNING OIL HYDRAULIC MOTOR	
10	JP 57209 547 A	<input checked="" type="checkbox"/>	COLLECTING DEVICE FOR PROGRAM EXECUTING CARRIER INFORMATION	
11	EP 23902 3 A1	<input checked="" type="checkbox"/>	Arrangement for processing branch instructions in pipelined data-processing systems.	
12	JP 20031 86663 A	<input checked="" type="checkbox"/>	Data processing system determines content to be corrected based on content transfer instructions and compares corrected content with selected data so as to notify correction completion state	
13	US 64053 07 B	<input checked="" type="checkbox"/>	Self modifying code conflict handling method in microprocessor, involves invalidating selected portion of information progressing through front end of IVE pipeline when contents of SAB matches with instruction pointer	
14	US 62725 61 B	<input checked="" type="checkbox"/>	Sound blaster interface card auto-detection method, involves identifying detection of card to be successfully completed on receiving an interruption	
15	GB 23453 54 A	<input checked="" type="checkbox"/>	Method of sound card interface auto detection	
16	US 56194 08 A	<input checked="" type="checkbox"/>	Instruction processing method for data processing system of superscalar, pipelined microprocessor - involves determining if selected instruction would be noneffective if executed by processor, and dispatching it to completion buffer if it does or recoding selected instruction, prior to dispatch to execution unit, if it does not	
17	EP 71636 4 A	<input checked="" type="checkbox"/>	Operator running support system for large scale e.g. nuclear, thermal or hydraulic power plant - compares guidance data operation instructions with selected output operation instructions to evaluate their correctness, with selected operation instructions being sent as control output when correct	
18	EP 46923 9 A	<input checked="" type="checkbox"/>	Detection and correction appts. for faulty processor operational codes - detects faulty instructions using logic nor circuit and replaces them with error-free micro-code from programmable array	
19	WO 91037 80 A	<input checked="" type="checkbox"/>	Controlling robot to prevent vibration in tip of its mechanism - determining current instruction value by adding correction torque found in selected operation expression to torque instruction value	

	Document ID	U	Title	Current OR
20	EP 30620 9 A	<input checked="" type="checkbox"/>	Dual rail processors with error checking at single rail interfaces - has shared resource devices coupled to processors for receiving data from output instructions from processors simultaneously	
21	US 44882 28 A	<input checked="" type="checkbox"/>	Virtual memory data processor - stores information relating to internal state upon detection of access fault during instruction execution	
22	JP 58182 113 A	<input type="checkbox"/>	Signal compensating device in decoding of digital signal - can selectively change instruction signal providing appropriate correction depending on detected burst length. NoAbstract Dwg 0/6	